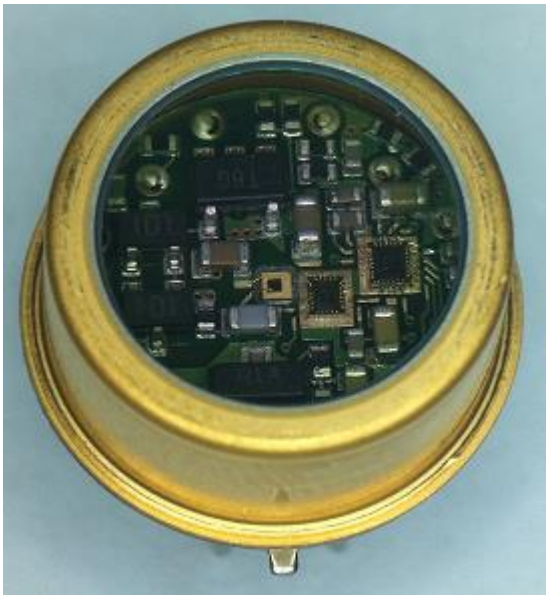
WOORIRO EYESAFE LASER RangeFinder RECEIVER

MODEL : WDR110

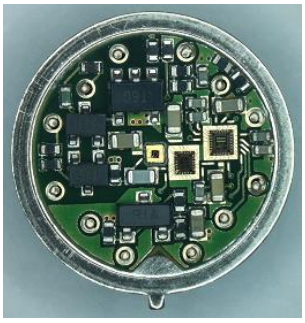


General Description

The Model WDR110 eyesafe LADAR receiver is released to be used for laser rangefinding and surveying. The InGaAs APD provides eye-safety and high sensitivity. CMOS IC is launched for more complex performance and compactness. Single FR4 PCB and standard TO-8 package provides a low cost solution for LADAR receiver.

Features

- 5ns~28ns input pulse
- InGaAs APD chip
- Integrated CMOS TIA and LOGIC
- CMOS logic output for detection (~15ns)
- Providing TPT(Time Programmed Threshold) mode
- Internally adjusted and temperature compensated APD bias
- Standard TO-8, FR4 PCB and quartz window for low cost application
- Single 3.3V power supply except APD bias
- High voltage of 80V for internally adjusted APD bias



Applications

- Low cost, low power consumption and high performance LADAR receiver

Absolute Maximum Ratings

Table 1. Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
TIA supply voltage	V_{DD}	+3.6	V
APD supply voltage(1)	V_{HV}	75	V
Optical input power(2)	P_{opt}	1	mW
Operating case temperature range	T_C	-32 to +64	℃
Storage temperature range	T_{STG}	-40 to +85	℃

(1) The minimum APD supply voltage must be larger than 70V for the proper biasing.

(2) WDR110 may be damaged permanently if the optical input power exceeding the rated value is applied. For long-term reliability, the maximum input power must be not to exceed 100uW.

Electro-Optical Characteristics

Inspection sheet shall be appended to products when they are delivered. Test report shall be submitted in papers and in electronic media. It shall contain the major in following items.

Table 2. Electro-Optical Characteristics (Tc=25°C)

Parameter		Performance	Condition
Type		Hybrid	
PD	Type	InGaAs APD	
	Diameter/Cap	200um/2.5 pF	
	Leakage current	Compensated	
	Position/tolerance	[TBD]	
Operating Wavelength		1550nm	
MDS (minimum detectable signal)		10 nW typ 15 nW max	@ 5ns pulse , MR=5A/W, SNR=3.3 (PD=50%, FAR=0.1%) Noise = 4.0mVrms max
Multiple target resolution		200 ns max	@ 100uW and 5ns pulse, successive pulses with same amplitude
Time programmed threshold		Enabled	External circuit needed
Dynamic Range		1:55,000	From noise level to 100uW.
Power consumption		3.3V / 17mA	
Output		CMOS with 15ns duration	
Walk error		10ns typ 20ns max	@ 5ns pulse
Weight		3g	

Functional Diagram

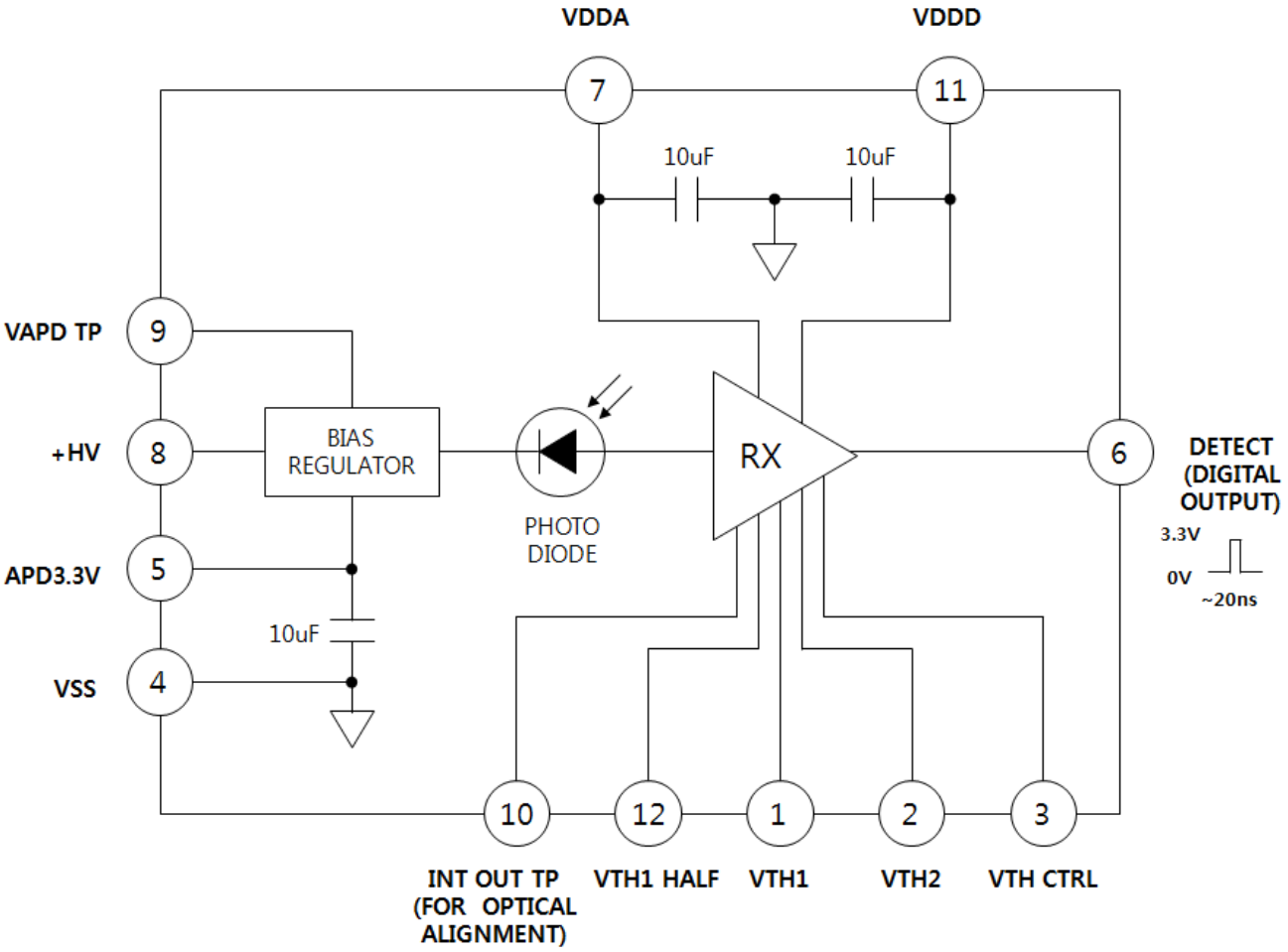


Figure 1. Functional block diagram

Pin Configuration

Table 3. PIN Configuration

Pin Number	Function	Description
1	VTH1	Control False Alarm Rate. External bypass capacitor 100pF is required.
2	VTH2	Control False Alarm Rate. External bypass capacitor 100pF is required.
3	VTH CTRL	Control TPG(Time Programmed Gain). External TPG circuits are required.
4	VSS	Ground.
5	APD3.3V	Power Supply Voltage for the APD Bias circuits. External bypass capacitors 10uF and 1uF are required.
6	DETECT	Digital CMOS Output pin with about 20ns duration and 3.3V positive pulse output when detect.
7	VDDA	Power Supply Voltage for the Analog circuits. External bypass capacitors 10uF and 1uF are required.
8	+HV	High Voltage VDD of APD Bias. +75V typ.
9	VAPD TP	VAPD Bias TP.
10	INT OUT TP	Integrator output TP. This pin is used for Optical Alignment.
11	VDDD	Power Supply Voltage for the Digital circuits. External bypass capacitors 10uF and 1uF are required.
12	VTH1 HALF	Control False Alarm Rate. External bypass capacitor 100pF is required.

Power On/Off Sequence

Not to damage the WDR110, the biasing sequence of HV(pin#8) and APD3.3V(pin#5) should be as following;

1. For power on, the DC power supply at APD3.3V(pin#5) should be connected first, and then HV(pin#8) applied.
2. For power off, the DC power supply at HV(pin#8) should be disconnected first, and then APD3.3V(pin#5) disconnected.

Application Circuit

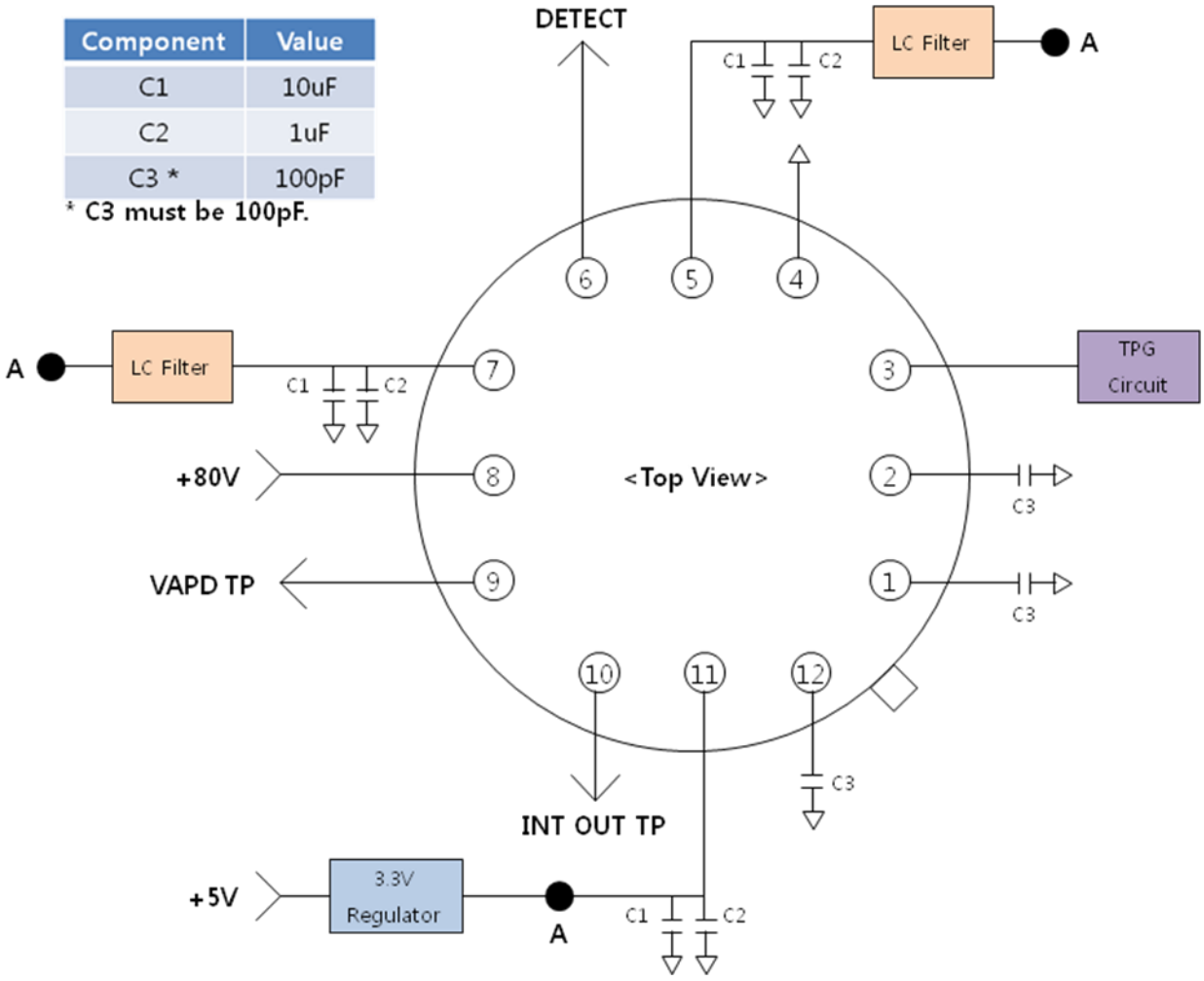
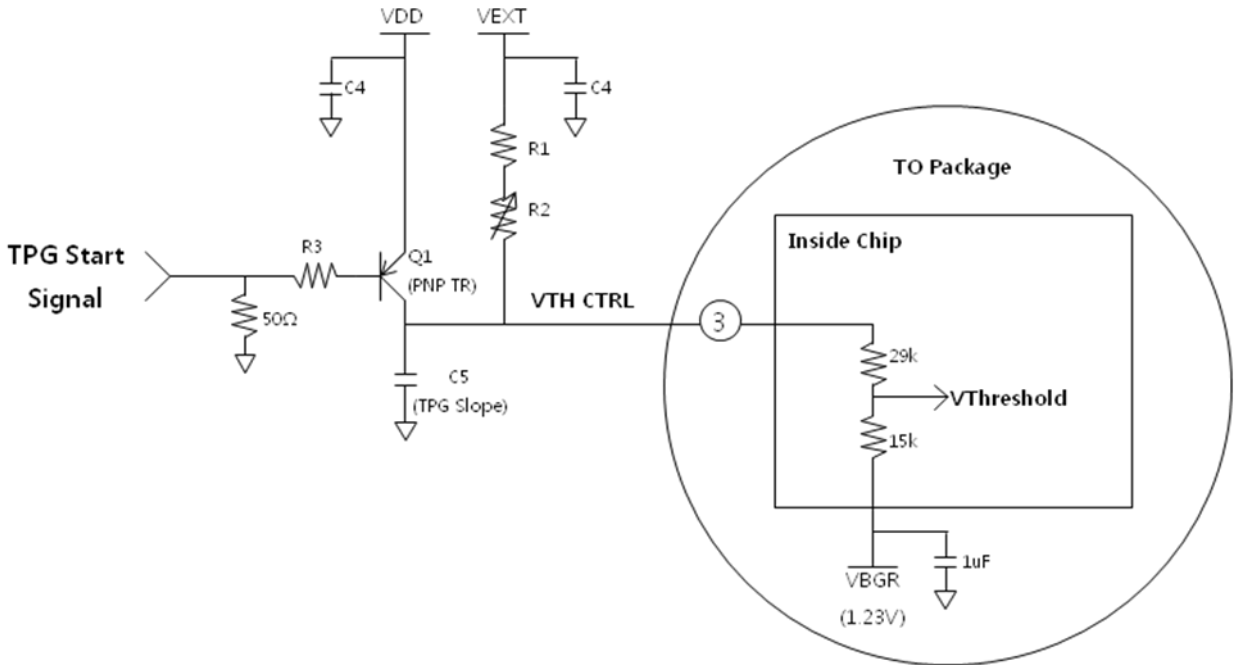
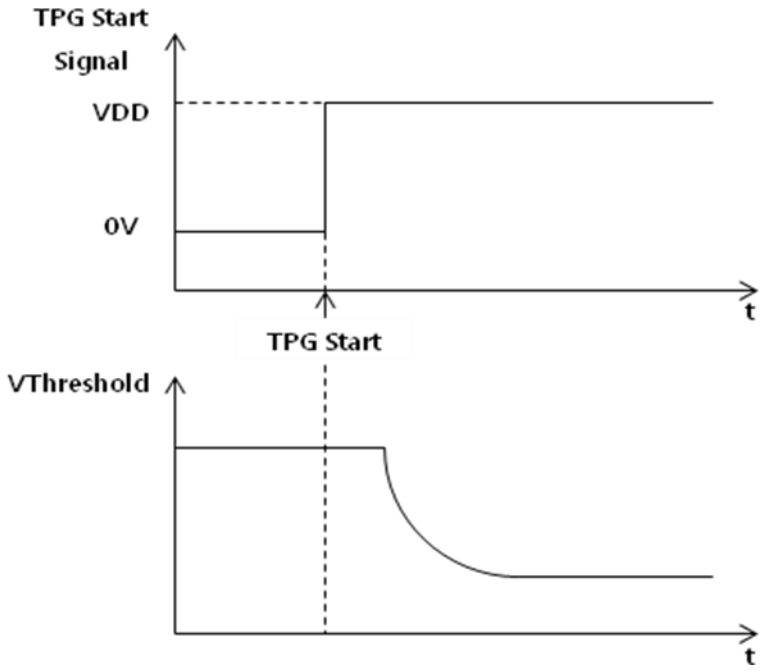


Figure 2. Application Circuit

Application Circuit (Continued)



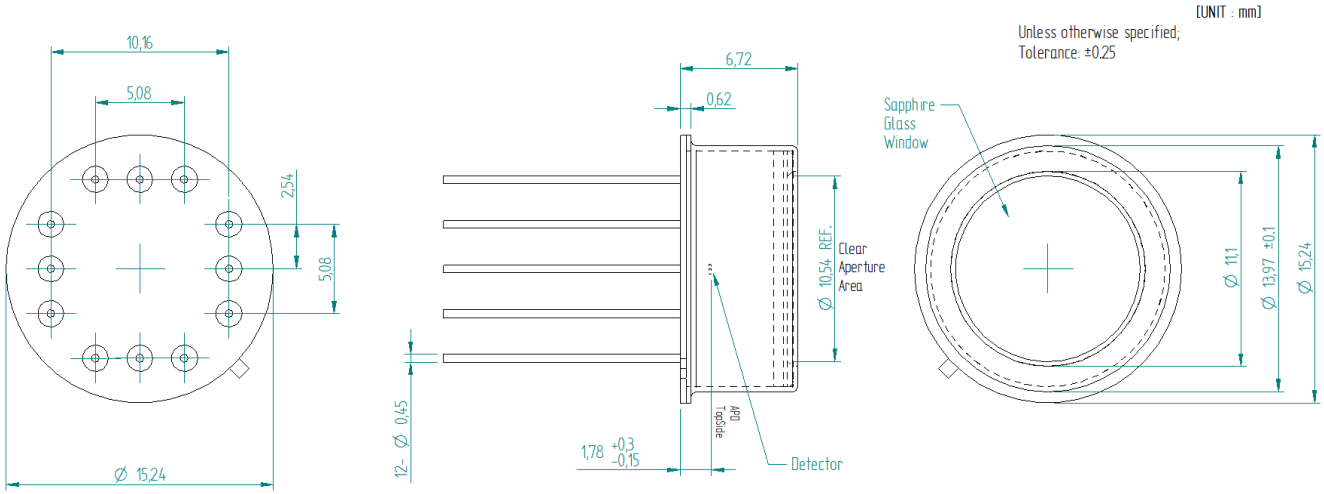
(a) Circuit Example



(b) Time Response

Figure 3. TPG (Time Programmed Gain) Circuit

Mechanical Dimension



Bottom View **Top View**

Figure 4. Mechanical Dimension

Precautions for Use

This device is susceptible to damage as a result of ESD(electrostatic discharge). Use of ground straps, anti static mats, and other standard ESD protective equipment is recommended when handling or testing this device. Soldering temperature of the leads should not exceed 350℃ for more than 10 seconds.